

Eng. Tech. College /Baghdad
Mechatronics Tech. Eng. Dept.
Academic Year 2017-2018
The Final Exam



Subject : Digital Logic Design
Class: First
Exam. Date: 4 / 6 / 2018
Allowed Time: 3 Hours

ملاحظة : الإجابة على جميع الأسئلة.

(15 Marks)

Q1/A/ Answer **Five** only from the following:

- 1- Convert the $(49)_{10}$ into its equivalent octal number.
- 2- What is the equivalent decimal value of $(111.011)_2$.
- 3- Find the Gray code of $(25)_{10}$.
- 4- What is the equivalent decimal value of $(29E)_{16}$.
- 5- Convert the $(46)_{\text{Excess-3}}$ code into its equivalent hexadecimal value
- 6- Use 9's complement arithmetic operation to perform $(355)_{10} - (142)_{10}$

(10 Marks)

B/ For the given Product-of-sum function $F(A, B, C, D) = \sum (1, 3, 4, 6, 9, 11, 12, 14)$,

Design a logic gates circuit to implement the given function using karnaugh map method.

(24 Marks)

Q2/ Answer **Three** only from the following :

- 1- Illustrate the design of even parity generator using two chips of multiplexer of 2-selectors to generate an even bit (p) for a 4-bit input (A, B, C, D).
- 2- Draw a 4-bit BCD Adder circuit and show the inputs and outputs of all logic circuit for input numbers A=1001 and B=0101 using comparator as detecting circuit.
- 3- Draw the circuit of 2's complement Add / Sub circuit, and then perform the following operations using the circuit, $(1001)_2 - (0100)_2$, $(1001)_2 + (0100)_2$

4- Drive the Boolean expression of full adder circuit and then draw the logic gates circuit of the driven expression .

(20 Marks)

Q3/ Design synchronous counter using J-K flip flop and present and next state method to count the following states : ($0 \rightarrow 1 \rightarrow 5 \rightarrow 6 \rightarrow 7$) , and then draw the output waveform of each flip flop.

(21 Marks)

Q4/A/ Explain with drawing the basic operation of the following (Answer Three only)

- 1- The logic gate and the truth table of gated D – Latch.
- 2- The logic blocks and the counting states of 4-bit Johnson shift counter.
- 3- The logic gates and the truth table of 2-selectors decoder.
- 4- The logic gates and the truth table of Demultiplexer of 2-selectors.

(10 Marks)

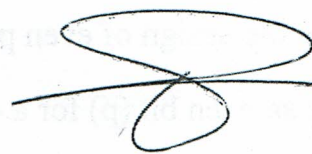
B/ Design Asynchronous counter for the following cases :

- 1- ($0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 8 \rightarrow 9$) using positive edge J-K flip flop.
- 2- ($8 \rightarrow 7 \rightarrow 6 \rightarrow 5 \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 0$) using negative edge J-K flip flop.



رئيس القسم

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مدرس المادة

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